Electrical and Electronics Engineering Lab Report

Exp No: *03*
Exp Name: ***Verification of Kirchhoff's Law***.
Equipmets: 1.Ammeter 2.Voltmenter 3.Bread borad 4.Three resistance 5.DC power supply 6.Connecting wires

Theory:

Kirchhoff's current law(KCL) states that the algebraic sum of current entering a node (or a closed boundary) is *zero*.

$$\sum_{n=1}^{N} i_n = 0$$

Kirchhoff's voltage law(KVL) states that the algebraic sum of all voltages around a close palth (or looop) is *zero*.

$$\sum_{m=1}^{M} V_m = 0$$

Circuit diagram of KCL: The circuit diagram is look like the following figure below.

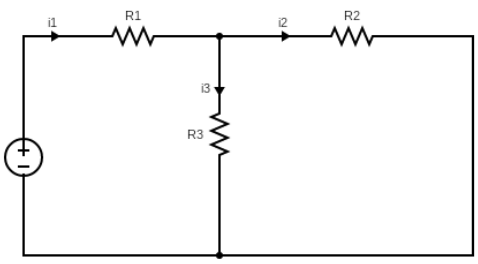

Fig 3.1: KCL Circuit diagram

Data table:

$s.n$	$voltage(V)$	I_1	I_2	I_3	$Error = \lvert\frac{I_1-(I_2+I_3)}{I_1}\rvert \times 100\%$
1	3	0.180	0.090	0.090	0%
2	4	0.250	0.120	0.120	4%
3	6	0.310	0.150	0.150	3.22%

Circuit diagram of KVL: The circuit diagram is look like the following figure below.

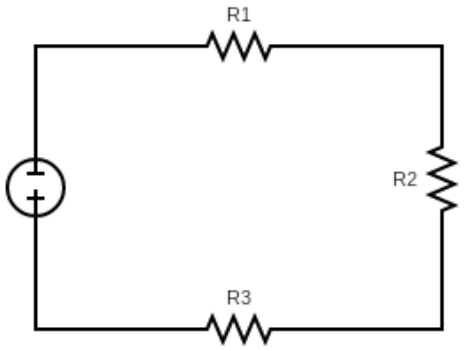

Fig 3.2: KVL Circuit diagram

Data table:

$s.n$	$Voltage(V_s)$	V_1	V_2	V_3	$Error = \lvert\frac{V_s-(V_1+V_2+V_3)}{V_s}\rvert \times 100\%$
1	3	0.998	0.963	0.998	1.367%
2	4	1.311	1.283	1.314	2.3%
3	6	1.65	1.621	1.668	1.22%

Result: The experimental results indicate that according to Kirchhoff's voltage lawtotal current of a loop and the sum of all currents following a node is equal to *zero*. There are some problems in electronics element of the experiment and these the cause of error.

Discussion: Kirchhoff's law is very essential law for electrical circuit. From this experiment we have verified the law if there works accuracy was better the input and out voltage would same and some would *zero*. Though there are a little error, we've verified this lawthere are a little error, we've verified this law.